## REMARKS

Claims 1-6 have been canceled. Claims 7-11 are pending in the application. Applicants amend claim 10 for further clarification, and refer to Figs. 15-16 and their corresponding description—including page 16, lines 34-37 and page 17, lines 14-17—in the specification for an exemplary embodiment of and support for the claimed invention. No new matter has been added.

Claims 7-8 and 10-11 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,901,136 to Lovelace et al.; and claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatenable over Lovelace et al. in view of U.S. Patent No. 6,081,569 to Hanson et al. Applicants amend claim 10 in a good faith effort to further clarify the invention as distinguished from the cited references, and respectfully traverse the rejections.

The Examiner relied upon the description in Lovelace et al. of a memory storage 74 as alleged disclosure of the claimed memories of a common part. The cited portions of Lovelace et al. only include, however, description of the memory storage 74 being coupled to "'A' and 'B' planes" of a control structure, and storing control and switch configuration information. Please see, e.g., Fig. 5 and its corresponding description—including col. 10, lines 23-31—in Lovelace et al. As such, Lovelace et al., as cited and relied upon by the Examiner, fail to disclose writing each frame output from interface parts into a memory in a common part, and a cross-connecting part reading out each frame from the memory(ies) in the common part so that the common part adjusts phases of frames output from the interface parts using the memory(ies).

In other words, Lovelace et al., as cited and relied upon by the Examiner, fail to disclose,

> "[a] transmission apparatus for cross-connecting channels on a synchronous multiplex transmission network, the transmission apparatus comprising interface parts and a

common part that includes a cross-connecting part and memories each corresponding to one of the interface parts,

each of the interface parts comprising:

a synchronous pulse generating part configured to generate a reference timing pulse that is synchronized among the interface parts; and

a frame generating part configured to generate a frame for synchronous multiplex transmission based on the reference timing pulse and outputs the frame to the common part,

wherein each frame output from the interface parts is written into one of the memories in the common part, and the cross-connecting part reads out each frame from the memories so that the common part adjusts phases of frames output from the interface parts using the memories," as recited in claim 10. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 10, together with claims 7-8 and 11 dependent therefrom, is patentable over Lovelace et al. for at least the foregoing reasons. The Examiner relied upon Hanson et al. as a combining reference to specifically address the additional features recited in dependent claim 9. As such, the addition of this reference would still have failed to cure the above-described deficiencies of Lovelace et al., even assuming, arguendo, that such an addition would have been obvious to one skilled in the art at the time the claimed invention was made. Accordingly, Applicants respectfully submit that claim 9 is patentable over the cited references for at least the foregoing reasons.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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